

FINAL EXAM PROJECT

Design a dc-dc converter with the following specifications:

- $V_g = 500 \text{ ?}700 \text{ V}$, $V_o = 300 \pm 1 \text{ V}$, $P_o = 10 \text{ ?}120 \text{ W}$;
- Isolation is not required, but it is allowed;
- $10 \text{ kHz} \leq f_s \leq 100 \text{ kHz}$;
- Maximum v_o high frequency ripple $< 0.5 \text{ V}$;
- Power dissipation on any switch or diode should not exceed 1 W in steady-state;
- Maximum deviation of v_o during transients is less than $\pm 30 \text{ V}$ and the settling time to within $\pm 0.5 \text{ V}$ of steady state is less than 10 ms . The transients are defined as:
 - v_g steps from 550 V to 650 V or reverse, with $|\partial v_g / \partial t| = 1 \text{ V}/\mu\text{s}$ and $P_o = 120 \text{ W}$;
 - i_o steps from 300 mA to 400 mA or reverse, with $|\partial i_o / \partial t| = 1 \text{ mA}/\mu\text{s}$ and $V_g = 600 \text{ V}$;
- Phase margin of at least 45° and the gain margin of at least 6 dB ;
- Minimize weight and cost.

1) Design the power stage, i.e. choose the switching frequency and find the values of inductors and power capacitors, and the number of windings and turns ratios of transformers (if used). Verify the design results by performing PSpice switching frequency transient simulations of the power stage without feedback (but with adjusted duty cycle so that $\langle v_o \rangle = 300 \pm 1 \text{ V}$). Use the following components in simulations:

- Sbreak switch model with $R_{OFF} = 10 \text{ M}\Omega$, $R_{ON} = 5 \Omega$, $V_{OFF} = 0 \text{ V}$, and $V_{ON} = 10 \text{ V}$, to model a high voltage switch;
- Dbreak diode model with $I_s = 10 \mu\text{A}$, $C_{jo} = 200 \text{ pF}$, and $R_s = 5 \Omega$ to model a high voltage diode;
- VPULSE voltage source model with $V_1 = -5 \text{ V}$, $V_2 = 15 \text{ V}$, $T_D = 0$, $T_R = 200 \text{ ns}$, and $T_F = 500 \text{ ns}$, to model a gate drive circuit;
- Standard 10% capacitors;
- Inductors and transformer turns ratios with two significant digits.

Show the following results:

- Complete circuit diagram of the converter, as simulated;
- Sbreak, Dbreak, and VPULSE model parameters used in simulations, either together with the circuit diagram or on a separate sheet;
- Four steady-state periods of the output voltage with sufficient detail to prove that you meet high frequency ripple requirement under all operating conditions;

- d. Four steady-state periods of currents and voltages on each switch and diode for the following operating conditions: $V_g = 500 \text{ V}$, $P_o = 120 \text{ W}$, and $V_g = 700 \text{ V}$, $P_o = 120 \text{ W}$;
- e. Steady-state dissipation in the switches and diodes by using the Probe function $\text{AVG}(v*i)$, where v and i are the voltage and current in a switch or diode.
- f. Four steady-state periods of currents in all inductors and transformer windings under the same operating conditions as in (d) above.

2) Design the magnetic devices. Use ferrite cores from Appendix 2 of the textbook with $B_{sat} = 0.5 \text{ T}$ and $\mu_r = 1500$, and copper wires from the same appendix with $J_m = 250 \text{ A/cm}^2$.

Show the following results:

- a. Selected core type, air-gap length, number of turns, selected AWG;
- b. Sketch to scale (two times enlarged) the cross section of the core and winding structure;
- c. Estimate the low-frequency loss in the magnetic devices by calculating the approximate dc resistance of all windings.

3) Design the voltage feedback control loop, i.e. find the values of all controller components. Verify the design results by performing PSpice ac and transient simulations of the converter average model with feedback. Use the following components in simulations:

- AwgPWMsw ideal PWM switch model with $F_s = \text{your switching frequency}$ and $L = \text{your main inductance}$ (Neglect all losses.);
- VDC voltage source with DC = 5.1 V, IOPAMP, and GAIN models as the average models of the necessary parts of UC3823 PWM controller (PWM ramp peak-to-peak voltage is $V_m = 1.8 \text{ V}$);
- Standard 5% resistors
- One 1 M Ω pot;
- Standard 10% capacitors;

Show the following results:

- a. Complete circuit diagram of the converter and the feedback, as simulated;
- b. Loop gain with clearly marked phase and gain margins for the following operating conditions: $V_g = 500 \text{ V}$, $P_o = 120 \text{ W}$, and $V_g = 700 \text{ V}$, $P_o = 10 \text{ W}$;
- c. Closed-loop transient simulations showing that you meet all the transient specifications.