

PROJECT #2

BUCK-BOOST CONVERTER CONTROL DESIGN

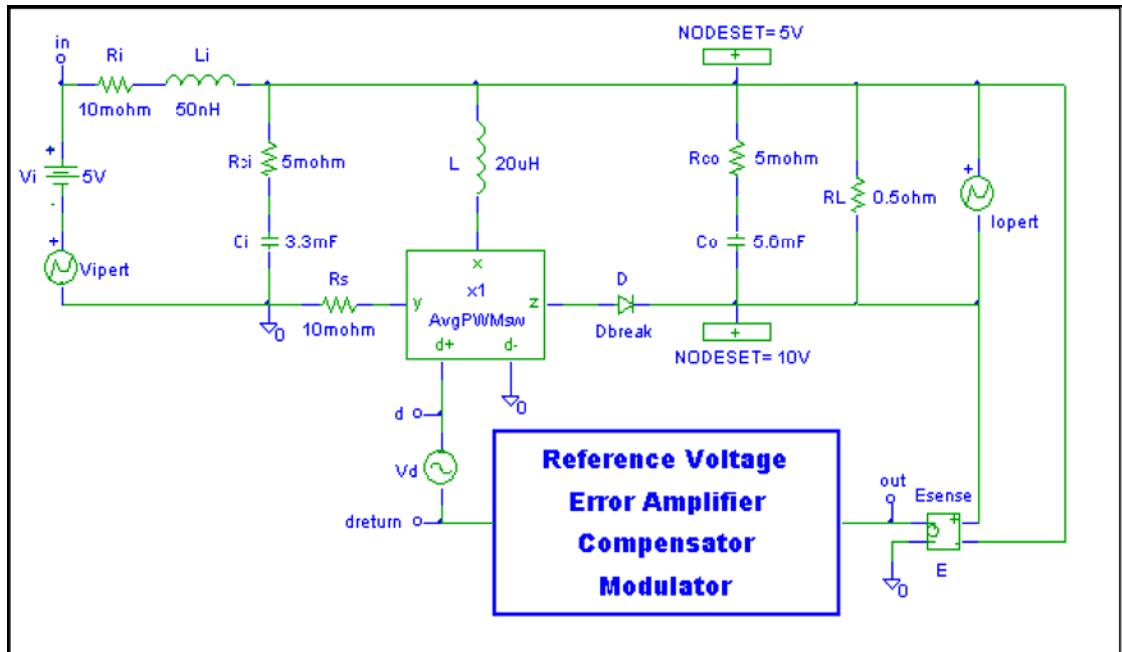


Fig. 1. Buck-boost converter PSpice simulation diagram.

Design the feedback circuit for the 50 W buck-boost converter shown above with the following nominal component values:

$$\begin{aligned}
 V_i &= 5 \text{ V}, & V_o &= 5 \text{ V} \pm 2 \%, & R_s &= 10 \text{ m}\Omega, \\
 R_i &= 10 \text{ m}\Omega, & R_L &= 0.5 \Omega, & f_s &= 40 \text{ kHz}, \\
 L_i &= 50 \text{ nH}, & L &= 20 \mu\text{H}, & V_{\text{ramp(p-p)}} &= 2 \text{ V}, \\
 R_{C_i} &= 5 \text{ m}\Omega, & R_{C_o} &= 5 \text{ m}\Omega, \\
 C_i &= 3.3 \text{ mF}, & C_o &= 5.6 \text{ mF},
 \end{aligned}$$

where R_s is the switch average resistance and $V_{\text{ramp(p-p)}}$ is the modulator saw-tooth peak-to-peak voltage. **You need to achieve the loop-gain cross-over frequency of $f_c \geq 1 \text{ kHz}$, phase margin of $\phi_m \geq 30^\circ$, and the gain margin of $G_m \geq 6 \text{ dB}$.**

Design the complete feedback circuit except for the modulator implementation, and find the values of all components. In your design, you are allowed to use only op-amps, standard 5 % resistors, standard 10 % capacitors, a single 10 k Ω pot with 1 Ω resolution, one 1N750 Zener diode, and one auxiliary power supply, $V_{cc} = 15 \text{ V}$. You are not allowed to combine resistors or capacitors in series or parallel to obtain more precise values.

Verify your results through simulations using average model of the buck-boost converter. You can use the average PWM switch model (AvgPwmSw) and idealized op-amp model

(IOPAMP) that are available in libraries. The model for the 1N750 diode is available in the PSpice EVAL libraries and the model Dbreak used for the power diode is in the PSpice BREAKOUT libraries. You will need to modify Dbreak model in the BREAKOUT.LIB file to use default diode resistance, Rs, as follows:

```
*$
.model Dbreak D Is=1e-14 Cj0=.1pF ; Rs=.1
*$
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Insert the semicolon!

The diode D in Fig. 1 often would not be used in the average analysis, because its switching function is already included in the average PWM switch model. However, it may be used (together with the switch resistance Rs) to obtain more realistic steady-state operating point values and the Q-factor value. The independent sources Vipert and lopert in Fig.1 are of the PWL (piecewise linear) type and are used to introduce AC and TRANSIENT perturbations at the circuit input and output. The source Vd in Fig. 1 is used to set the duty-cycle dc value in the open-loop analysis, as well as to introduce AC perturbations for both open-loop and closed-loop analyses. The dependent source Esense is used to differentially sense the output voltage. For the closed-loop simulations it is often necessary to help PSpice find the DC operating point by specifying an initial guess using NODESET1 elements (available in the PSpice SPECIAL.SLB library), as shown in Fig. 1.

The report should contain the following:

- a) Outline of your design and all calculated component values.
- b) Circuit diagram as used in simulations.
- c) Magnitude (dB) and phase plots, each on a single diagram with two Y-axes and with X-axis from 1 Hz to 100 kHz (min. 20 points per decade), of the following transfer functions (TFs):
 - duty-cycle to output TF, $g(f) \equiv V(\text{out})/V(\text{d})$, with Vipert = lopert = 0, and Vd = (AC);
 - compensator TF, $h(f) \equiv V(\text{dreturn})/V(\text{out})$, with Vipert = lopert = 0, and Vd = (AC);
 - loop gain, $l(f) \equiv V(\text{dreturn})/V(\text{d})$, with Vipert = lopert = 0, and Vd = (AC);
 - open-loop audio-susceptibility, $a(f) \equiv V(\text{out})/V(\text{in})$, with Vipert = (AC), lopert = 0, Vd = (DC), and dreturn connected to ground (You may need to insert a resistor in series with the feedback output before shorting it to ground.);
 - open-loop output impedance, $Z_o(f) \equiv V(\text{out})/I(\text{loper})$, with Vipert = 0, lopert = (AC), Vd = (DC), and dreturn connected to ground;
 - closed-loop audio-susceptibility, $a_{CL}(f)$;
 - closed-loop output impedance, $Z_{oCL}(f)$.

(Use same Y-axis scaling factors for open- and closed-loop plots of audiosusceptibility and output impedance.)
- d) Closed-loop transient plots of V(in), I(RL) + I(loper), V(d), I(L), and V(out) when Vopert and lopert change as shown in Fig. 2, and Vd = 0. The total simulation time should be 200 ms and the maximum step size should not be larger than 0.5 ms.

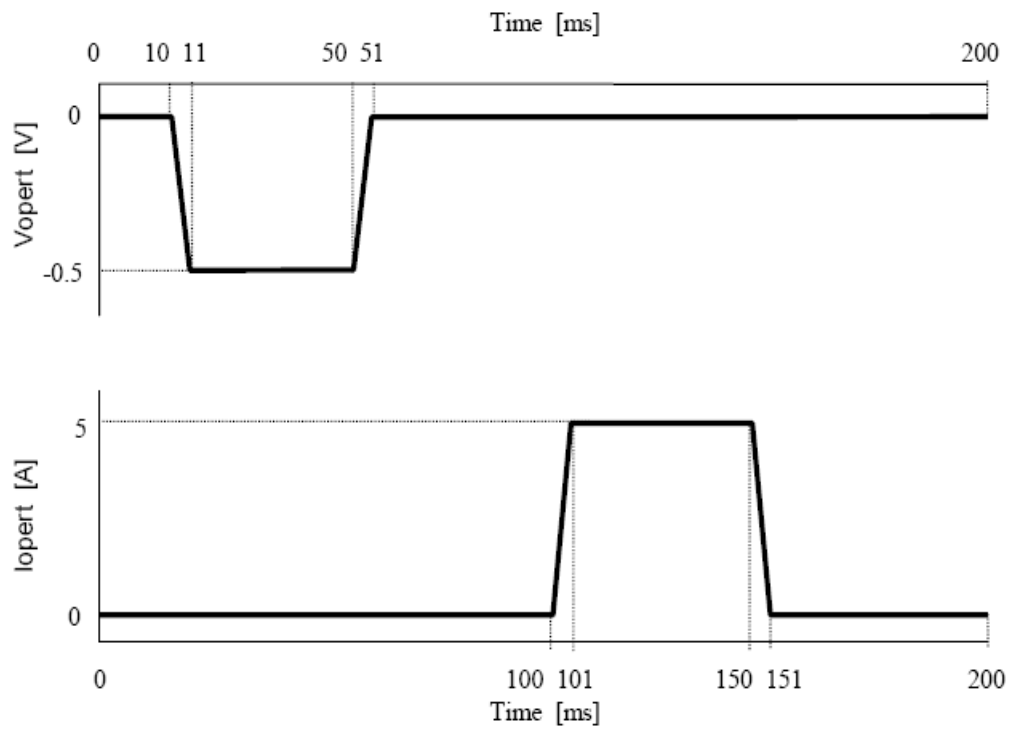


Fig. 2. Waveforms of input voltage and load current disturbance for transient analysis.