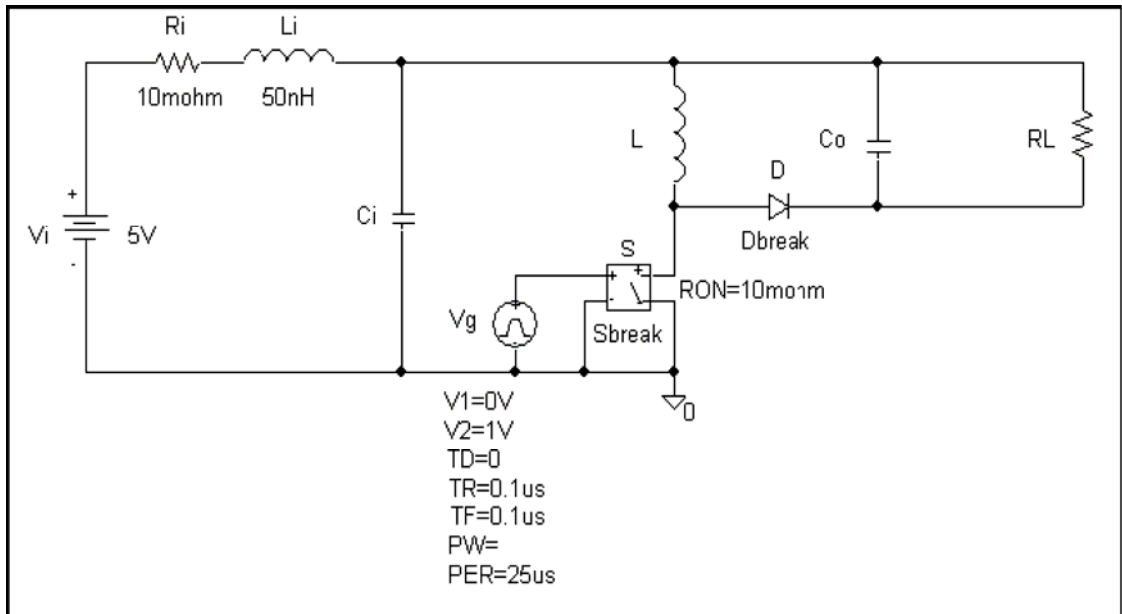


PROJECT #1

BUCK-BOOST CONVERTER POWER STAGE DESIGN



Design the power stage of the 50 W buck-boost converter shown above for the following specifications:

- $V_i = 5\text{ V}$, $V_o = 5\text{ V} \pm 2\%$,
- $R_i = 10\text{ m}\Omega$, $\Delta v_o \leq 30\text{ mV}$,
- $L_i = 50\text{ nH}$, $f_s = 40\text{ kHz}$.
- $\Delta v_{C_i} \leq 50\text{ mV}$,

The voltage drop across the diode when conducting is $V_{DON} \approx 0.9\text{ V}$, and the switch ON resistance is $R_{SON} \approx 10\text{ m}\Omega$. Find the values of:

- Steady state duty cycle, D ,
- Switch rms current, $I_{S_{rms}}$,
- Inductance, L ,
- Switch power dissipation, P_S ,
- Input capacitance, C_i ,
- Diode peak voltage, V_{Dp} ,
- Output capacitance, C_o ,
- Diode average current, I_D ,
- Peak inductor current, I_{Lp} ,
- Diode power dissipation, P_D ,
- Switch peak voltage, V_{Sp} ,
- Efficiency, $\eta \equiv P_o / (P_o + P_S + P_D + P_{Ri})$.

You need to show your design procedure and reasoning. Use approximate analysis from the class. You may want to use more precise analysis only for finding the duty cycle, D , to save you simulation time later. Your design must meet all the specs, but it must not be an overkill, i.e. you should not use capacitor values larger than 10 mF, and inductor value larger than 1 mH, and your voltage ripples should not be smaller than half of the specified maximum values. In your design, you are allowed to use inductor values with only one significant digit and standard 10 % capacitor values.

Verify your results through simulations using **Sbreak** and **Dbreak** models from the PSpice **Breakout** library. You will need to modify **Dbreak** model in the **Breakout.lib** file to use default diode resistance, R_s , as follows:

```
*$  
.model Dbreak D Is=1e-14 Cj0=.1pF ; Rs=.1  
*$
```

insert the semicolon!

We are interested now only in the steady state response. Therefore, your simulations need to reach approximate steady state. Use initial conditions for C's and L's to shorten the simulation time. Adjust the duty cycle, D , as necessary to get the output average voltage within $5\text{ V} \pm 2\%$.

The report should contain the following:

- a) Outline of your design and all calculated values required above.
- b) Circuit diagram as used in simulations.
- c) Steady state waveforms during four switching periods for the following variables:
 - $v(L)$ & $i(L)$ - $v(C_i)$ & $i(C_i)$
 - $v(S)$ & $i(S)$ - $v(C_o)$ & $i(C_o)$
 - $v(D)$ & $i(D)$ - $i(L_i)$ & $i(R_L)$.

Show all the waveforms on separate plots, but two plots per page, in pairs as given above. Use the same horizontal scale for all plots and appropriate vertical scaling to show necessary details.